

FIG. 1

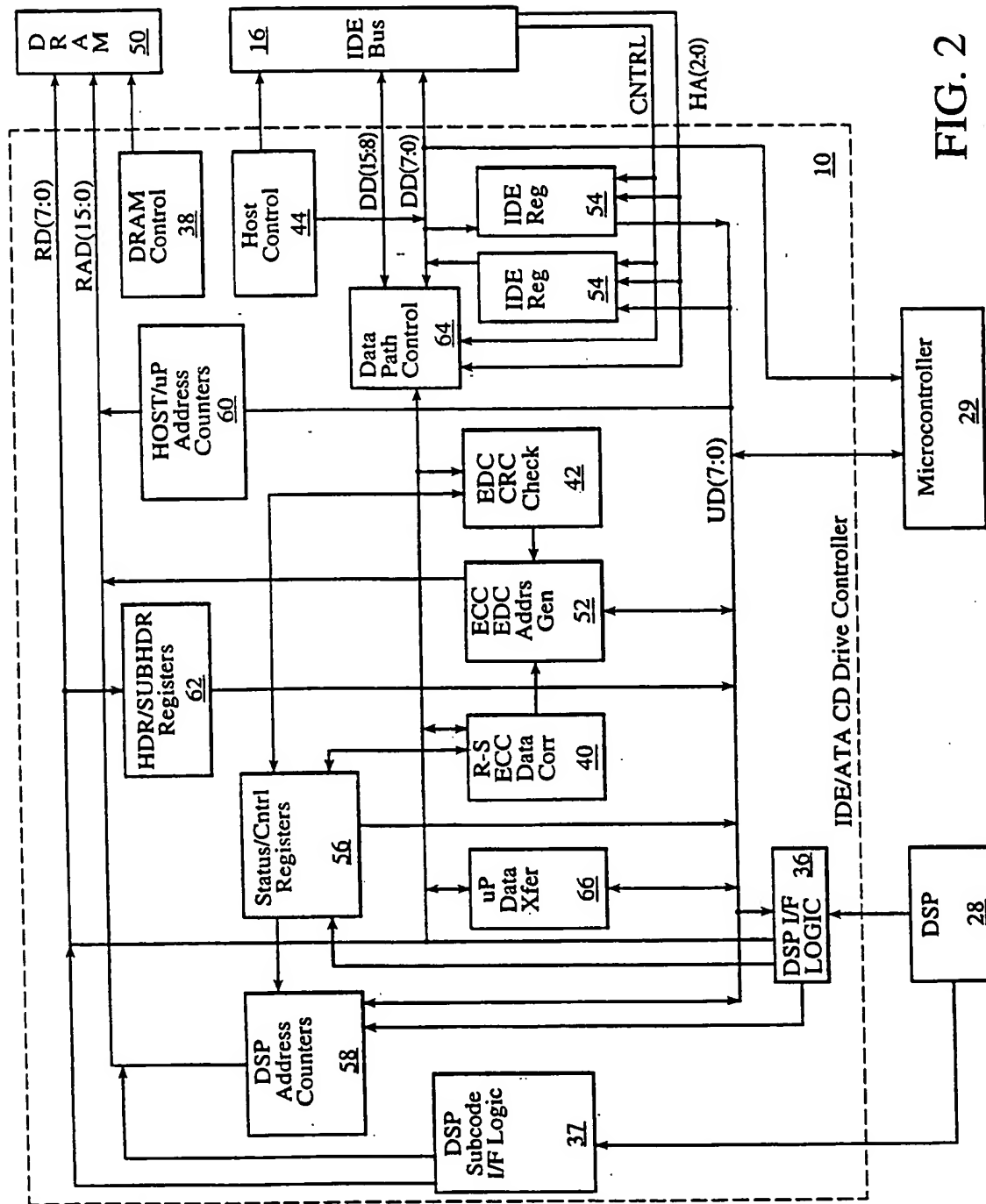


FIG. 2

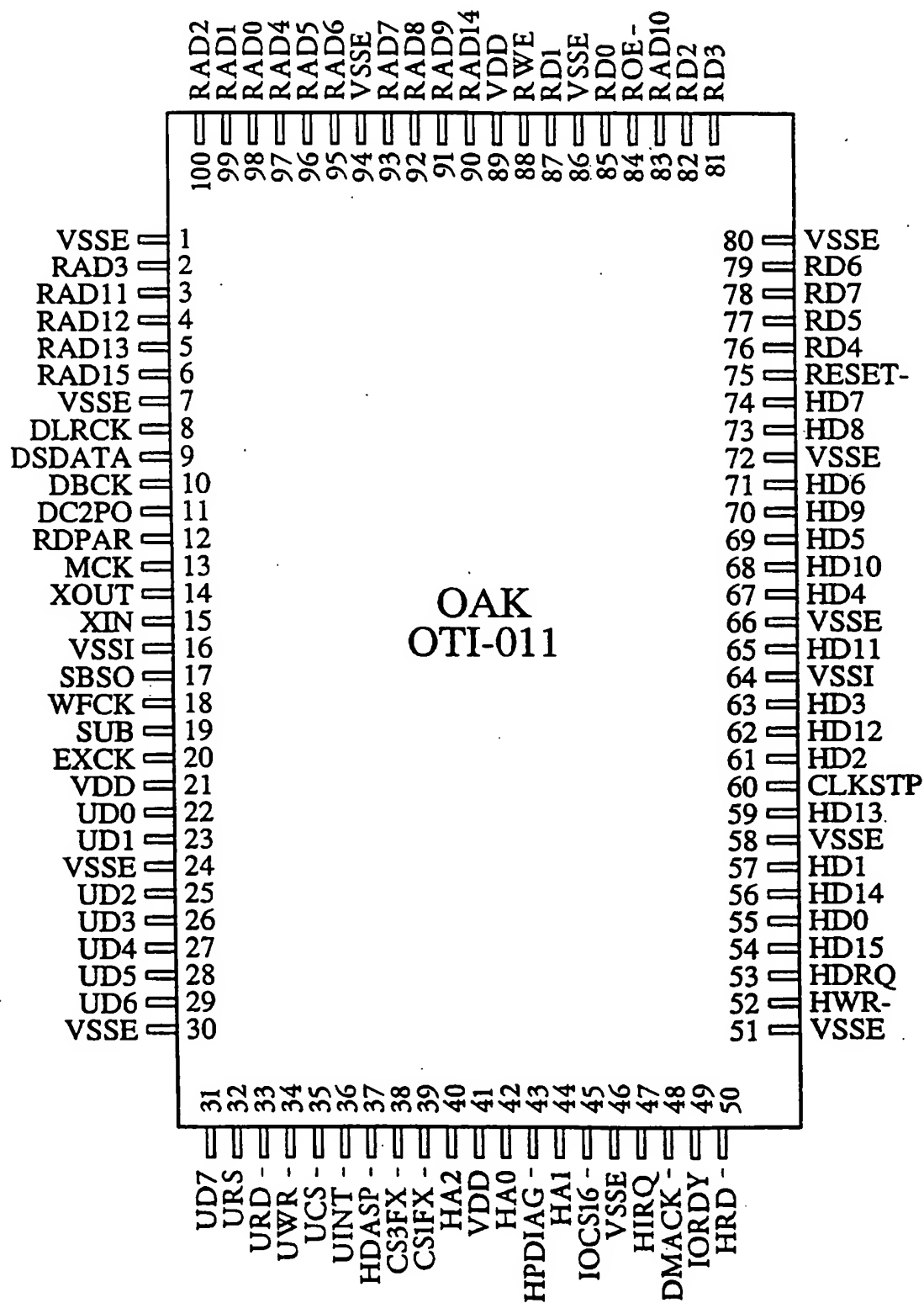


FIG. 3a

Pin#	Pin Name	Type	Comments	Pin#	Pin Name	Type	Comments
1	VSSE	P		29	UD6	B	uCOM Data Bus
2	RAD3	O	RAM Address Bus	30	VSSE	P	
3	RAD11	O		31	UD7	B	uCOM Data Bus
4	RAD12	O		32	URS	I	uCOM Register Select
5	RAD13	O		33	URD-	I	uCOM Read Strobe
6	RAD15	O		34	UWR-	I	uCOM Write Strobe
7	VSSE	P		35	UCS-	I	uCOM Chip Select
8	DLRCK	I	44.1KHz L/R Strobe	36	UINT-	O	uCOM Interrupt
9	DSDATA	I	Serial Data	37	HDASP-	B	IDE Host Interface
10	DBCK	I	Serial Bit Clock	38	CS3FX	I	
11	DC2PO	I	C2 Pointer Input	39	CS1FX	I	
12	RDPAR	B	RAM Parity Data	40	HA2	I	
13	MCK	O		41	VDD	P	
14	XOUT	O	X'tal OSC Output	42	HAO	I	IDE Host Interface
15	XIN	I	X'tal OSC Input	43	HPDIAG-	B	
16	VSSI	P		44	HA1	I	
17	SBSO	I	Subcode Interface	45	IOCS16-	O	
18	WFCK	I		46	VSSE	P	
19	SUB	I		47	HIRQ	O	IDE Host Interface
20	EXCK	B		48	DMACK-	I	
21	VDD	P		49	IORDY	O	
22	UDO	B	uCOM Data Bus	50	HRD-	I	
23	UD1	B		51	VSSE	P	
24	VSSE	P		52	HWR-	I	IDE Host Interface
25	UD2	B	uCOM Data Bus	53	HDRQ	O	
26	UD3	B		54	HD15	B	
27	UD4	B		55	HD0	B	IDE Host Data Bus
28	UD5	B		56	HD14	B	

FIG. 3b

Pin#	Pin Name	Type	Comments	Pin#	Pin Name	Type	Comments
57	HD1	B	IDE Host Data Bus	79	RD6	B	RAM Data Bus
58	VSSE	P		80	VSSE	P	
59	HD13	B	IDE Host Data Bus	81	RD3	B	RAM Data Bus
60	CLKSTP	I		82	RD2	B	
61	HD2	B	IDE Host Data Bus	83	RAD10	O	RAM Address Bus
62	HD12	B		84	ROE-	B	RAM Read Enable
63	HD3	B		85	RDO	B	RAM Data Bus
64	VSSI	P		86	VSSE	P	
65	HD11	B	IDE Host Data Bus	87	RD1	B	RAM Data Bus
66	VSSE	P		88	RWE-	O	RAM Write Enable
67	HD4	B	IDE Host Data Bus	89	VDD	P	
68	HD10	B		90	RAD14	O	RAM Address Bus
69	HD5	B		91	RAD9	O	
70	HD9	B		92	RAD8	O	
71	HD6	B		93	RAD7	O	
72	VSSE	P		94	VSSE	P	
73	HD8	B	IDE Host Data Bus	95	RAD6	O	RAM Address Bus
74	HD7	B		96	RAD5	O	
75	RESET-	I		97	RAD4	O	
76	RD4	B	RAM Data Bus	98	RAD0	O	
77	RD5	B		99	RAD1	O	
78	RD7	B		100	RAD2	O	

FIG. 3c

Pin Name	Pin Type	Pin Description
UD7-UD0	I/O	uCONTROLLER DATA BUS - Microcontroller bidirectional data bus. This bus is compatible with most microcontrollers.
URS-	IN	uCONTROLLER REGISTER SELECT - Register select input. AR (address register) is selected if URS=0. Otherwise, microcontroller will access the internal register that is pointed by the AR register.
URD-	IN	uCONTROLLER READ STROBE - Microcontroller read strobe.
UWR-	IN	uCONTROLLER WRITE STROBE - Microcontroller write strobe.
UCS-	IN	uCONTROLLER CHIP SELECT - Microcontroller chip select input.
UINT-	OUT/ Open-Drain	uCONTROLLER INTERRUPT - Microcontroller interrupt output. This is an open-drain output. This signal can be externally wired - OR with other interrupt sources.

FIG. 4

Pin Name	Pin Type	Pin Description
HD15 - HD0	I/O	HOST DATA BUS - Host Bidirectional Data Bus.
HWR-	IN	HOST WRITE STROBE - Host IO write strobe.
HRD-	IN	HOST READ STROBE - Host IO read strobe.
HA2-HA0	IN	HOST ADDRESS - These are the 3-bit Host Addresses asserted by the host to access a register or data port in the OTI-011.
IOCS16-	OUT/ Open-Drain	DRIVE 16-bits I/O - For PIO transfer, IOCS16- indicates to the host system that the 16-bit data port has been addressed and OTI-011 is prepared to send or receive 16-bit data word.
CS1FX-	IN	HOST CHIP SELECT 1 - This is the chip select signal decoded from the host address bus used to-select the Command Block registers in the OTI-011.
CS3FX-	IN	HOST CHIP SELECT 3 - This is the chip select signal decoded from the host address bus used to select the Control Block registers in the OTI-011.
HDRQ	OUT	HOST DMA REQUEST - This signal will be asserted for DMA data transfer when OTI-011 is ready to transfer data to or from the host. This signal is used in a handshake manner with DMACK-. When a DMA operation is enabled, data transfers are 16-bits wide.
DMACK-	IN	HOST DMA ACKNOWLEDGE - This signal is used by the host in response to HDRQ.
HIRO	OUT	HOST INTERRUPT - This signal is used to interrupt the host system.
IORDY	OUT	HOST IO READY - This signal is asserted to extend the host transfer cycle of any host read access when the OTI-011 is not ready to respond to a request.
HDASP-	I/O	HOST DRIVE ACTIVE/DRIVE 1 PRESENT - This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present. This signal is controlled by the firmware.
HPDIAG-	I/O	HOST PASSED DIAGNOSTICS - This signal is asserted by Drive 1 to indicate to Drive 0 that it has completed diagnostics. This signal is controlled by the firmware.

FIG. 5a

Addresses					Functions	
CS1FX-	CS3FX-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
					Control block registers	
N	N	x	x	x	Data bus high impedance	Not Used
N	A	1	1	0	Alternate ATAPI status	Device control
N	A	1	1	1	Drive Address	Not Used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	ATAPI Error Register	ADAPI Features
A	N	0	1	0	ATAPI Interrupt Reason Register (R/W)	
A	N	0	1	1	Not Used	Not Used
A	N	1	0	0	ATAPI Byte Count Register (bit 7-0) (R/W)	
A	N	1	0	1	ATAPI Byte Count Register (bit 15-8) (R/W)	
A	N	1	1	0	Drive Select (R/W)	
A	N	1	1	1	ATAPI Status	ATA Command
A	A	x	x	x	Invalid address	Invalid Address

Logic conventions are: A = signal asserted, N = signal negated

FIG. 5b

Pin Name	Pin Type	Pin Description
DSDATA	IN	DSP SERIAL DATA - This serial input receives the data from DSP (CIRC decoder). The DBCK pin provides the data clock to the OTI-011. The received data are stored in the buffer RAM.
DBCK	IN	DSP BIT CLOCK - This clock input receives bit clock from DSP.
DLRCK	IN	DSP L/R CLOCK - Supplies the signal which is used to distinguish L-channel/R-channel (44.1KHz) DLRCK signal also indicates the start timing of 16 bit PCM word.
DC2PO	IN	DSP C2 POINTER - Supplies C2 error flag signal from DSP. When high, DC2PO indicates an error condition.

FIG. 6

Pin Name	Pin Type	Pin Description
SBSO	IN	SUBCODE SERIAL DATA - Supplies Subcode serial data. The subcode words (P-W) will be stored into buffer RAM in the order.
SUB	IN	SUBCODE SYNC - Supplies Subcodes SYNC from DSP.
EXCK	I/O	EXTERNAL CLOCK - Supplies Bit Clock for Subcode interface. This pin can be programmed as input or output.
WFCK	IN	WRITE FRAME CLOCK - Supplies Write Frame Clock from DSP. (7.35KHz)

FIG. 7

Pin Name	Pin Type	Pin Description
RAD15- RAD0	OUT	RAM ADDRESS BUS - Buffer RAM address outputs.
RDPAR	I/O	RAM PARITY DATA - RAM Parity bit when RPEN = 1.
RD7 - RD0	I/O	RAM DATA BUS - Buffer RAM data bus.
RWE-	OUT	RAM WRITE ENABLE - The OTI-011 forces this pin low when writing data to the RAM.
ROE-	OUT	RAM OUTPUT ENABLE - The OTI-011 forces this pin low when reading data from the RAM.

FIG. 8a

Pin Name	Pin Function	Note
RA0 - RA8	DRAM address	
RA9		Left Open (see note)
RA10	CAS-	
RA11 - RA13		Left Open (see note)
RA14	RAS-	
RA15		Left Open (see note)

FIG. 8b

Miscellaneous Pins

Pin Name	Pin Type	Pin Description
XIN XOUT	IN OUT	XTAL INPUT/XTAL OUTPUT - XIN, XOUT are normally connected to a crystal. (up to 21MHz) XIN pin may be driven by the external signal. (21 MHz max. 45-55% duty) The OTI-011 contains an internal resister between XIN and XOUT, so that an external resister shall not be connected to these pins.
MCK	OUT	M CLOCK - This output supplies clock signal of one-half the crystal frequency when register bit MCK1 is low. When register bit MCK1 is high, MCK pin supplies crystal frequency.
CLKSTP	IN	CLOCK STOP - CLKSTP stops the internal clock, when it is high.
RESET-	IN	RESET - Forcing this input low reset the OTI-011. OTI-011 can be reset by either this reset signal or the internal reset command (Writing RESET register). RSSTAT register shows user which reset most recently took place.
VDD		Supplies 5.0V +/- 5%
VSSE/VSSI		Ground Pins

FIG. 9

AR - Address Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
-	R	address							
-	W	address							

FIG. 10

COMIN - Command Packet Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
00h	R	binary							
00h	W	unused							

FIG. 11

IFSTAT/IFCTRL - Interface Status Register/Interface Control Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
01h	R	cmdib	dteib	decib	X	dtbsyb	X	dtenb	X
01h	W	cmdien	deteien	decien	0	0	0	douten	0

FIG. 12

DBCL - Data Byte/Word Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
02h	R	b7	b6	b5	b4	b3	b2	b1	b0
02h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 13

DBCH - Data Byte/Word Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
03h	R	dtei	dtei	dtei	dtei	b11	b10	b9	b8
03h	W	0	0	0	0	b11	b10	b9	b8

FIG. 14

HEAD0/DACL - Header Register 0/Data Address Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
04h	R	header minutes (bcd)							
04h	W	a7	a6	a5	a4	a3	a2	a1	a0

FIG. 15

HEAD1/DACL - Header Registers/Data Address Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
05h	R	header seconds (bcd)							
05h	W	a15	a14	a13	a12	a11	a10	a9	a8

FIG. 16

HEAD2/DTTRG - Header Registers/Data Transfer Trigger									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
06h	R	header frames (bcd)							
06h	W	(data unused)							

FIG. 17

HEAD3/DTACK - Header Registers/Data Transfer Acknowledge									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
07h	R	header mode (bcd)							
07h	W	(data unused)							

FIG. 18

STARTING POINT	MODE 1 (MODRQ=0)	MODE 2 (MODRQ=1)
First Sync Byte	FF,F0h	FF,E8h
First Header Byte	FF,FCh	FF,F4h
First Subheader Byte	-	FF,F8h
First User Data Byte	00,00h	00,00h

FIG. 19

PTL/WAL - ECC Block Pointer/Write Address Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
08h	R	a7	a6	a5	a4	a3	a2	a1	0
08h	W	a7	a6	a5	a4	a3	a2	a1	a0

FIG. 20

PTH/WAH - ECC Block Pointer/Write Address Counter									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
09h	R	a15	a14	a13	a12	a11	a10	a9	a8
09h	W	a15	a14	a13	a12	a11	a10	a9	a8

FIG. 21

WAL/CTRL0 - Write Address Counter/Control 0 Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Ah	R	a7	a6	a5	a4	a3	a2	a1	0
0Ah	W	decen	0	e0lrq	autorq	0	wrrq	qrrq	prq

FIG. 22

DECEN 0Ah.7	WRRQ 0Ah.2	E0LRQ 0Ah.5	QRQ 0Ah.1	PRQ 0Ah.0	DECODER OPERATION	CRCOK (0Ch.7)	HEAD0-3, SUBHO-3 (04-07h,14-17TH)
1	1	1	1	1	Q-P-correction	Valid	Buffer RAM
1	1	1	1	0	Q-correction	Valid	Buffer RAM
1	1	1	0	1	P-correction	Valid	Buffer RAM
1	1	x	0	0	Write-only (no ECC)	Valid	Buffer RAM
1	0	x	0	0	Disk-monitor	Invalid	Incoming data
1	0	x	x	1	Not recommended		(see note)
1	0	x	1	x	Not recommended		(see note)
0	x	x	x	x	Decoder disabled	Invalid	Invalid

FIG. 23

WAH/CTRL1 - Write Address Counter/Control 1 Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Bh	R	a15	a14	a13	a12	a11	a10	a9	a8
0Bh	W	syien	syden	dscrlen	cowren	modrq	formrq	mbckrq	shdren

FIG. 24

STAT0/PTL - Status 0 Register/ECC Block Pointer									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Ch	R	crcok	ilsync	nosync	lblk	wshort	sblk	0	uceblk
0Ch	W	a7	a6	a5	a4	a3	a2	a1	a0

FIG. 25

SYIEN 0Bh.7	SYDEN 0Bh.6	SYNC OPERATION	ILSYNC 0Ch.6	NOSYNC 0Ch.5	LBLK 0Ch.4	SBLK 0Ch.2
1	1	Sync-insertion +detection	active	active	inactive	inactive
1	0	Sync-insertion only	inactive	active	inactive	active
0	1	Sync-detection only	active	inactive	active	inactive

FIG. 26

RMO3 0Eh.7	RMOD2 0Eh.6	RMOD1 0Eh.5	RMOD0 0Eh.4	MODE
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	$\langle 8*N \rangle + 0$
1	0	0	1	$\langle 8*N \rangle + 1$
1	0	1	0	$\langle 8*N \rangle + 2$
1	0	1	1	$\langle 8*N \rangle + 3$
1	1	0	0	$\langle 8*N \rangle + 4$
1	1	0	1	$\langle 8*N \rangle + 5$
1	1	1	0	$\langle 8*N \rangle + 6$
1	1	1	1	$\langle 8*N \rangle + 7$ or error

FIG. 29

STAT1/PTH - Status 1 Register/ECC Block Pointer									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Dh	R	0	0	0	hdera	0	0	0	shdera
0Dh	W	a15	a14	a13	a12	a11	a10	a9	a8

FIG. 27

STAT2/SFCTRL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Eh	R	rmod3	rmod2	rmod1	rmod0	mode	nocor	rform1	rform0
0Eh	W	unused							

FIG. 28

STAT3/RESET									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0Fh	R	valstb	0	cblk	0	0	0	0	0
0Fh	W	(data unused)							

FIG. 30

CTRLW									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
10h	R	unused							
10h	W	0	swen	sdss	dclke	0	0	0	0

FIG. 31

CRTRG									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
11h	R	unused							
11h	W	0	0	0	0	0	0	0	ctrl

FIG. 32

Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
12h	R	unused							
12h	W	unused							

FIG. 33

Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
13h	R	unused							
13h	W	unused							

FIG. 34

SUBH0									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
14h	R	subheader file number							
14h	W	unused							

FIG. 35

SUBH1									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
15h	R	subheader channel number							
15h	W	unused							

FIG. 36

SUBH2									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
16h	R	subheader submode number							
16h	W	unused							

FIG. 37

SUBH3									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
17h	R	subheader coding information							
17h	W	unused							

FIG. 38

DECODER OPERATION	REGISTER	ERASURE BYTE #	STORED BYTE #
Disk-monitor	SUBH0	no erasures	incoming byte 16
Disk-monitor	SUBH0	byte 16	incoming byte 20
Disk-monitor	SUBH0	byte 16 and 20	incoming byte 20
Buffered	SUBH0	don't care	buffered byte 20
Disk-monitor	SUBH1	no erasures	incoming byte 17
Disk-monitor	SUBH1	byte 17	incoming byte 21
Disk-monitor	SUBH1	byte 17 and 21	incoming byte 21
Buffered	SUBH1	don't care	buffered byte 21
Disk-monitor	SUBH2	no erasures	incoming byte 18
Disk-monitor	SUBH2	byte 18	incoming byte 22
Disk-monitor	SUBH2	byte 18 and 22	incoming byte 22
Buffered	SUBH2	don't care	buffered byte 22
Disk-monitor	SUBH3	no erasures	incoming byte 19
Disk-monitor	SUBH3	byte 19	incoming byte 23
Disk-monitor	SUBH3	byte 19 and 23	incoming byte 23
Buffered	SUBH3	don't care	buffered byte 23

FIG. 39

VER/XTAL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Ah	R	b7	b6	b5	b4	b3	b2	b1	b0
1Ah	W	0	0	0	0	mck1	0	0	xtald2

FIG. 40

DSPSL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Bh	R	unused							
1Bh	W	c2ml	sel16o	1chl	0	0	sel16	dir	edge

FIG. 41

UD7 c2ml	UD6 sell6o	UD5 lchl	UD4 X	UD3 X	UD2 sell6	UD1 dir	UD0 edge	DSP Type
1	0	1	0	0	0	1	0	Sony CXD1135Q
1	1	0	0	0	0	1	1	Philips SAA7345
0	0	1	0	0	1	0	0	Sanyo LC7860K
0	0	0	0	0	1	1	1	Toshiba
0	0	1	0	0	1	0	1	Matsushita MN66261

FIG. 42

HCON/UACL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Ch	R	unused							
1Ch	W	a7	a6	a5	a4	a3	a2	a1	a0

FIG. 43

DSPSL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Bh	R	unused							
1Bh	W	c1ml	sell6o	lchl	x	x	sell6	dir	edge

FIG. 44

HCON/UACL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Ch	R	0	spare	spare	spare	dts	sdrqb	lohi	dma16
1Ch	W	a7	a6	a5	a4	a3	a2	a1	a0

FIG. 45

UACH									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Dh	R	unused							
1Dh	W	a15	a14	a13	a12	a11	a10	a9	a8

FIG. 46

UACU									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Dh	W	0	0	0	0	b3	b2	b1	b0

FIG. 47

RAMRD/RAMWR									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Eh	R	rr7	rr6	rr5	rr4	rr3	rr2	rr1	rr0
1Eh	W	rw7	rw6	rw5	rw4	rw3	rw2	rw1	rw0

FIG. 48

HDDIR									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1Fh	R	urtbsy	cs13	0	0	0	0	hrwr	0
1Fh	W	udtrg	udata	host16	0	1	1	0	0

FIG. 49

Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	1	1	0	0

FIG. 50

HICTL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
20h	W	0	pdiagen	daspen	clrbsy	setbsy	scod	iordyen	iocsl6en

FIG. 51

SUBC2									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
21h	W	0	0	0	0	nopq	cdsp2	cdsp1	cdsp0

FIG. 52

CDSP2 21h.2	CDSP1 21h.1	CDSP0 21h.0	Subcode Block Rate
0	0	0	1X (75 blocks/sec)
0	0	1	2X (150 blocks/sec)
0	1	0	4X (300 blocks/sec)
1	0	0	Reserved

FIG. 53

STATS									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
22h	R	data unused					missy	sbkend	silsy
22h	W	data unused							

FIG. 54

DBACL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
24h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 55

DBACH									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
25h	W	0	0	0	0	0	0	0	b8

FIG. 56

SBKL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
26h	RW	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 57

SBKH									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
27h	RW	data unused							b8

FIG. 58

WBKL									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
28h	RW	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 59

WBKH									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
29h	RW	data unused							b8

FIG. 60

RAMCF									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Ah	R	rftyp	ramclr	ram0	uhilo	rpen	rcf2	rcf1	rcf0
2Ah	W	rftyp	ramclr	0	uhilo	rpen	rcf2	rcf1	rcf0

FIG. 61

RCF2 2Ah.2	RCF1 2Ah.1	RCF0 2Ah.0	RAM Configuration
0	0	1	128K DRAM (256K X 4-bit X 1)
0	1	0	256K DRAM (256K X 4-bit X 2)

FIG. 62

MEMCF - Memory Layout Configuration Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Bh	W	0	0	0	0	purg	iordyf	mly1	mly0

FIG. 63

MLY1 2Bh.1	MLY0 2Bh.0	DRAM Memory Layout Configuration
0	0	Data Blocks + Last 2 Auxiliary/Subcode Blocks
1	1	Data Blocks + All Auxiliary/Subcode Blocks

FIG. 64

SUBCD - Subcode Control									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Ch	W	sbxck	scen	scbk2	scien	exinv	exop	sbsel1	sbsel0

FIG. 65

SBSEL1 2Ch.1	SBSEL0 2Ch.0	Subcode Format
0	0	SMD0 (Philips)
0	1	SMD1 (EIAJ-1)
1	0	SMD2 (EIAJ-2)
1	1	Undefined

FIG. 66

UMISC - Miscellaneous Microcontroller Control									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Eh	R	1	1	1	1	1	1	pdiagb	daspb
2Eh	W	ideien	0	drveb	drv1b	hintrq	0	0	0

FIG. 67

RSSTAT - Reset, IDE, and Subcode Status Register									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
2Fh	R	srst	cmd	diagcmd	sint	parint	rst	urst	hrst

FIG. 68

ATFEA/ATERR									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
31h	R	0	0	0	0	0	0	0	dma
31h	W	b7	b6	b5	b4	mcr	abrt	eom	ili

FIG. 69

ATINT									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
32h	RW	0	0	0	0	0	0	io	cod

FIG. 70

ATSPA									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
33h	RW	0	0	0	0	0	0	0	1

FIG. 71

ATBLO									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
34h	RW	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 72

ATBHI									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
35h	RW	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 73

ATDRS									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
36h	RW	1	1	1	drv	0	0	0	0

FIG. 74

ATCMD/ATSTA									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
37h	R	b7	b6	b5	b4	b3	b2	b1	b0
37h	W	0	drdy	0	drc	drq	corr	0	check

FIG. 75

DFIF0									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
40h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 76

DFIF1									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
41h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 77

DFIF2									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
42h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 78

DFIF3									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
43h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 79

DFIF4									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
44h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 80

DFIF5									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
45h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 81

DFIF6									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
46h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 82

DFIF7									
Address	Type	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
47h	W	b7	b6	b5	b4	b3	b2	b1	b0

FIG. 83